AMENDMENTS TO THE SPECIFICATION

Please amend the fourth paragraph on page 4 to read as follows:

~~FIGs. 3A-3C~~ FIGS. 3A-3D are cross-sectional drawings illustrating a method ~~for~~ of forming a thin, planarized layer of polysilicon in accordance with the present invention.

Please amend the fifth paragraph on page 4 to read as follows:

~~FIGs. 3A-3C~~ FIGS. 3A-3D show cross-sectional drawings that illustrate a method ~~for~~ of forming a thin, planarized layer of polysilicon in accordance with the present invention. As shown in FIG. 3A, the method utilizes a conventionally processed semiconductor wafer 300 that has a top surface 310. Surface 310, in turn, has a number of substantially-equal lower levels 312 and a number of substantially-equal upper levels 314 that lie above the lower levels 312.

Please amend the third paragraph on page 5 as follows:

After this, as shown in FIG. 3B, oxide layer 330 and polysilicon layer 320 are chemically-mechanically polished until oxide layer 330 is substantially, completely removed from the surface of polysilicon layer 320 to form a planarized layer of polysilicon 340. Once planarized layer of polysilicon 340 has been formed, as shown in FIG. 3C, a mask ~~(not shown)~~ 341 is formed and patterned on planarized polysilicon layer 340.

Please amend the fifth paragraph on page 5 (which continues on to page 6) as follows:

Alternately, after the planarization step, one or more additional layers of materials, such as materials which lower the resistance of polysilicon, can be formed over layer 340. As shown in FIG. ~~3C~~ 3D, a layer of material 342 ~~that lowers resistance~~ is formed over planarized polysilicon layer 340. ~~The mask~~ Mask 341 is then formed and patterned on the additional layers of material (e.g., layer 342) which are then etched along with planarized polysilicon layer 340 to form the structures (e.g., local interconnect lines). Either way, once the structures have been formed, the method continues with conventional back-end processing steps.